

USB 2.0 Device Core

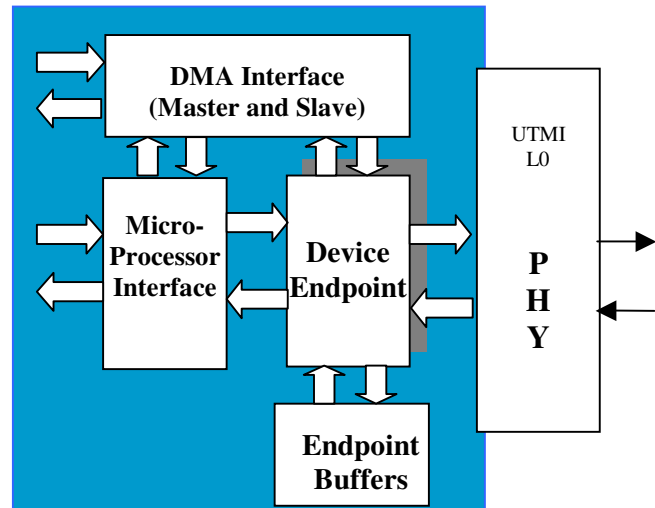
Introduction

The SPCUSB20 is a functional core for devices implementing USB 2.0. It provides all the features that are necessary to implement a USB device on SOC design. This core provides high speed DMA interface, which can be configured as a master or slave. The SPCUSB20 supports a maximum of 15 configurable endpoints and it provides support for generic 8/16-bit, 8051, 80x86, AHB Processor interfaces. This Core requires an external USB 2.0 UTMI Macro Cell for full chip integration.

Features

- USB 2.0 compliant
- Backward Compatibility with USB 1.1 (FS only)
- External USB 2.0 UTMI Macro cell I/F.
- 15 configurable endpoints, excluding Control endpoint.
- Control Endpoint (2 x 16 B or 2 x 64 Bytes).
- Configurable Bulk / Interrupt / Isochronous Endpoints.
- Bulk Endpoint (2 x 64 / 512B or 3 x 64 / 512B)
- Isochronous Endpoint (2 x 1024B / 3 x 1024B).
- Configurable Endpoint Buffer depth.
- Integrated HS DMA interface (Master/Slave)
- 8 bit 60 MHz / 16 bit 30 MHz UTMI Interface.
- DMA Master-Block Mode Support.
- DMA Slave-Byte & Block Mode Support.
- Variable DACK / Strobe Width.

Block Diagram



Applications

- DSL Modems.
- ATA / ATAPI Interface.
- Digital Cameras.
- Printers.
- Scanners.
- Networking.
- Digital Media Controllers.
- Video Transport.

Architecture

Highlights of the architecture are as follows

UTMI Interface: This block handles USB reset, suspend and resume detection. During packet reception, it decodes the incoming token, performs crc check and deposits the data encoded within the USB packet into the Endpoint buffers. During transmit operation; it packetizes the endpoint data in USB format.

Processor Interface: This block allows the CPU access to the device specific configuration, control and status registers. It provides a generic interface to 8/16-bit processors. In addition 8051, 80x86 and AHB processor interfaces are supported as well.

Endpoint buffers: These buffers can be configured for double buffering or triple buffering. The application data received or to be transmitted to the USB host is stored in endpoint buffers.

DMA Interface: This provides a programmable DMA master / slave interface to external application for accessing data from the endpoint buffers.

Deliverables

- **Verilog RTL Source.**
- **Complete Test suite in HVL VERA**
- **Processor Model, UTMI BFM with Monitor**
- **PERL -TK based configurator.**
- **Sample Firmware for USB protocol layer.**
- **Hardware / Programmer's Manual.**

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